CLAIMS

1. A method for location of a fault of the short-circuit type, of a logic gate, known as the defective logic gate, of an integrated circuit, known as the defective circuit, comprising a chip, input terminals and output terminals connected to one another by electrically conductive tracks, and logic gates formed within the chip of the circuit, which is generally in the form of a wafer which defines a main plane of the chip, the tracks extending in the thickness of the chip or on the surface, globally parallel to the main plane, the input and output terminals being connected to the tracks at the periphery of the chip, and at least two electrical energy supply terminals with direct voltage (VDD-VSS), at least one supply terminal of which is connected to a high potential VDD, and at least one supply terminal of which is connected to a low potential VSS, in which:

- a sequence of distinct vectors, known as location vectors, is created and recorded, each of which is formed from a series of signals, which are designed to be able to be applied to the different input terminals of the defective circuit;
- for at least one location vector applied to the input terminals of the defective circuit and/or of an integrated circuit, known as the standard circuit, which is free from a defective gate and from any fault, and is also identical to the defective circuit, a set of images, known as vector images, is produced and recorded, representing equipotential lines formed by the tracks and the logic gates of the said circuit, each equipotential line corresponding to one of the differentiated states of potential on the vector images, the different vector images of a single set of images being designed to cover and represent the entire surface of the chip, or an entire portion of this surface on which it is being attempted to locate the defective logic gate;

wherein:

- each location vector is formed from binary signals which assume one of the logic states 0 and 1, and maintain this logic state throughout an entire period, in which it is considered that the location vector is applied to the input terminals, such that this sequence can be applied step by step, one location vector after the other, and keeping each location vector applied for a period which is as long as necessary at the input terminals of the defective circuit and/or of a standard circuit, without the electric state of this circuit changing during this period;
- the sequence of location vectors is applied step by step to the input terminals of the defective circuit, and for each location vector, measurement is made of the value IDDQ(j) of the electrical consumption current at rest IDDQ of the defective circuit, which is circulating in at least one of the supply terminals, and it is determined whether this value measured IDDQ(j) is normal or abnormal, and the result of this determination is recorded;
- at least one location vector, known as the abnormal location vector, is applied to the input terminals of the defective circuit and/or of a standard circuit, for which the fact has

previously been determined and recorded that the value measured IDDQ(j) of the electrical consumption current at rest IDDQ of the defective circuit is abnormal, and a set of images, known as abnormal vector images, of the said circuit with this abnormal location vector is produced and recorded; and

- in a further step of location of the defective gate, at least one comparison is made between at least one abnormal vector image (70, 76, 81, 89) and another pre-recorded image, known as the reference image (71, 77, 82, 88), corresponding to the same portion of surface of the chip of the defective circuit or of the standard circuit as the abnormal vector image, these images being selected such that this comparison makes it possible to select an area, known as the defective area, of the surface of the chip on which there can be located an equipotential input line (73, 93) of the defective logic gate and/or an equipotential output line (74, 87, 92) of the defective logic gate, and/or the defective logic gate.

2. A method as claimed in claim 1, wherein:

- in a first step, the sequence of location vectors is created and recorded;
- in a second step, there is application step by step of the sequence of location vectors, to the input terminals of the defective circuit, the value IDDQ(j) is measured of the electrical consumption current at rest IDDQ of the defective circuit, for each location vector, it is determined whether the location vector is abnormal, and this information is recorded;
- in a third step, there is selection and recording from amongst the sequence of location vectors, of a list of location vectors which is designed to produce the vector images which make it possible to locate the defective gate by comparison;
- in a fourth step, there is application, sequentially, step by step, of the list of location vectors, to the input terminals of the defective circuit and/or of a standard circuit, and a set of vector images for the location vectors of this list is produced and recorded; and
- in a fifth step, the step of location of the defective gate is carried out by using the vector images produced in the fourth step.

3. A method as claimed in claim 1 or claim 2, wherein the sequence of location vectors is created such that each location vector is formed by binary signals with the format NRZ, which maintain the same logic state 0 or 1, until a subsequent location vector is applied to the input terminals, or, if the final location vector is involved, until completion of the measurement(s) and production of image(s) carried out for this location vector.

4. A method as claimed in claims 1 to 3, wherein the sequence of location vectors is created from a sequence of vectors, known as test vectors, which is previously formed and recorded, and is designed to make it possible to determine the existence only of a defective

gate in the defective circuit, by measurement of the value of the electrical consumption current at rest IDDQ of the defective circuit, and each test vector for which the binary signal of at least one input terminal is liable to change its logic state, is broken down into a plurality of location vectors, the logic state of the binary signals of which does not change.

5. A method as claimed in any one of claims 1 to 4, wherein the sequence of location vectors is created such that two consecutive location vectors are distinguished from one another by the value of a single binary signal applied to a single input terminal.

6. A method as claimed in any one of claims 1 to 5, wherein, in order to measure the value of the electrical consumption current at rest IDDQ of the defective circuit, at least one supply terminal of the defective circuit is applied to the input of an amplifier circuit (23) which is fitted as a current/voltage converter.

7. A method as claimed in claim 6, wherein the supply terminal of the defective circuit which is connected to a low potential VSS is used, and the amplifier circuit (23) fitted is a current/voltage converter, and is designed to create a virtual memory, which is adjustable according to the constraints imposed by the supply of the integrated circuit on which the value of the current IDDQ is measured.

8. A method as claimed in claim 7, wherein it is determined whether the value measured IDDQ(j) is normal or abnormal, by comparing it with a known nominal electrical consumption current at rest IDDQnom of the defective circuit.

9. A method as claimed in any one of claims 1 to 7, wherein it is determined whether the value measured IDDQ(j) is normal or abnormal, by calculating the standardised difference:

$$D=[IDDQ(j)-IDDQ^{0}(j)]/maximum[IDDQ^{0}(j),Imin]$$

in which

IDDQ(j) is the value measured of the electrical consumption current at rest IDDQ, of the defective circuit with the test vector j;

$IDDQ^{0}(j)$ is the value measured of the electrical consumption current at rest IDDQ, of a standard circuit; and

Imin is a minimum current value which is pre-determined in order to eliminate the effects of noise, the value IDDQ(j) being considered to be abnormal if D is greater than a pre-determined threshold value DS.

10. A method as claimed in claim 9, wherein DS is selected between 2 and 100.

Sub A3

11. A method as claimed in any one of claims 1 to 10, wherein, after a first comparison has been made, in which at least one defective area of the surface of the chip has been selected, at least one further comparison is made, only from vector images which correspond to the said defective area.

12. A method as claimed in any one of claims 1 to 11, wherein, for an abnormal location vector, a comparison is made of two sets of images of the defective circuit and/or of a standard circuit, at least one of the two sets of images being a set of vector images which is obtained with the said abnormal location vector, such as to select a defective area in which the defective logic gate can be located, and a further comparison is subsequently made only with the sets of vector images which represent the said defective area.

13. A method as claimed in any one of claims 1 to 12, wherein, during a first comparison of the step of location of the fault, the abnormal vector image used for the image is at least one vector image of a set of vector images, obtained with the first abnormal location vector appearing first in the sequence of location vectors.

14. A method as claimed in any one of claims 1 to 13, wherein the electrical functionality of the defective circuit is tested, and, if the defective circuit is found to be non-functional as far as one output terminal at least is concerned, as the reference image, use is made of a vector image, known as the fault reference image (71), obtained with the defective circuit for a location vector, known as the normal location vector, for which the value measured of the consumption current at rest IDDQ of the defective circuit, is normal.

15. A method as claimed in claim 13 and claim 14, wherein the fault reference image (71) used is a vector image which is obtained with the defective circuit, in the same sequence of location vectors, with a location vector which precedes the abnormal location vector.

16. A method as claimed in claim 14 and claim 15, wherein, for a comparison, the abnormal vector image used is a vector image, known as the fault abnormal vector image (70), of the defective circuit, and, in order to compare the fault abnormal vector image (70) and the fault reference image (71), an image is formed, known as the simple fault input image (72, 72'), representing the equipotential lines of the defective circuit which have the same form and the same location, and states of potential which differ between the fault abnormal vector image (70) and the fault reference image (71), such as to be representative of the equipotential input line of the defective logic gate.

17. A method as claimed in claim 16, wherein a plurality of simple fault input images (72, 72') is formed from a single fault abnormal vector image (70), which is compared with a plurality of fault reference images (71), and an image is formed, known as the intersection fault input image (75), representing the equipotential lines which are common amongst the different simple fault input images (72, 72').

18. A method as claimed in any one of claims 14 to 17, wherein, during the step of location of the defective gate, at least one comparison is made between two images of a standard circuit formed from an abnormal vector image, known as the standard abnormal vector image (76), obtained by applying an abnormal location vector to this standard circuit, and from a reference image, known as the standard reference image (77), obtained by applying a normal location vector to the standard circuit.

19. A method as claimed in claim 18, wherein, on the basis of the standard abnormal vector image (76) and the standard reference image (77), an image is formed, known as the simple standard input/output image (78, 78'), representing the equipotential lines of the standard circuit which have the same form and the same location, and states of potential which differ between the standard abnormal vector image (76) and the standard reference image (77), such as to be representative of the equipotential input line and the equipotential output line of the defective logic gate of the defective circuit.

20. A method as claimed in claim 19, wherein a plurality of simple standard input/output images (78, 78') is formed from a single standard abnormal vector image (76), which is compared with a plurality of standard reference images (77), and an image is formed, known as the intersection standard input/output image (79), representing the equipotential lines which are common amongst the different simple standard input/output images (78, 78').

21. A method as claimed in claim 16 or claim 17, and claim 19 or claim 20, wherein, during a further comparison, an image is formed, known as the output image (80), representing the equipotential lines which appear on a simple fault input image (72, 72') or on an intersection fault input image (75), or on a simple standard input/output image (78, 78'), or on an intersection standard input/output image (79); with the exclusion of the equipotential lines which are common amongst these images, this output image (80) representing the equipotential output line of the defective logic gate, and its propagation in the defective circuit.

22. A method as claimed in claim 21, wherein there is division of an intersection (75) or simple (72, 72') fault input image and an output image (80) representing the same portion of surface of the chip, in adjacent rectangular windows which have the same pre-determined fixed dimensions, which are smaller than those of these images (72, 72', 75, 80), for each window it is examined whether each of the two images (72, 72', 75, 80) does or does not have at least one equipotential line, and the window(s) having at least one equipotential line in each of these two images (72, 72', 75, 80) is/are selected and recorded.

23. A method as claimed in any one of claims 1 to 13, wherein the electrical functionality of the defective circuit is tested, and, if the defective circuit is found to be functional for all the output terminals, a comparison is made between at least one first abnormal vector image (81) obtained with a first abnormal location vector, and at least one second abnormal vector image (82) obtained with the same circuit, and with a second abnormal location vector which is distinct from the first abnormal location vector, the first and second abnormal location vectors belonging to the same sequence of location vectors.

24. A method as claimed in claim 23, wherein an image is formed, known as the fault output image (83), representing the equipotential line(s) which is/are common to the different abnormal vector images (81, 82), comprising the equipotential output line (87) of the defective logic gate.

25. A method as claimed in claim 24, wherein, in a further comparison, an image is formed, known as the intermediate output image (85), representing the equipotential lines which appear in common on the fault output image (83) and on at least one normal vector image (84) obtained with a normal location vector, with the exclusion of the equipotential lines which are common to this fault output image (83) and this normal vector image (84), the said intermediate output image (85) comprising the equipotential output line (87) of the defective logic gate.

26. A method as claimed in claim 24 and claim 25, wherein, in a further comparison, an image is formed, known as the output image (86), which represents the equipotential lines common to the fault output image (83) and to the intermediate output image (85), the said output image (86) representing the equipotential output line of the defective logic gate.

27. A method as claimed in any one of claims 1 to 26, wherein the test images are produced by electronic scanning microscopy with contrast of potential, by detection of the secondary electrons.

28. A method as claimed in any one of claims 1 to 27, wherein the vector images are recorded in monochrome pixelised form, and each comparison is made between images in pixelised form, numerically, pixel by pixel.

29. A method as claimed in claim 28, wherein, before using an image in an image comparison step, this image is previously integrated onto a plurality of identical exposures which correspond to this image, and median filtering is carried out by allocating to each pixel the median value of the series of pixels comprising this pixel and the pixels which surround it, such as to eliminate the peaks caused by the noise.

30. A method as claimed in claim 28 or claim 29, wherein, in order to form an image representing the equipotential lines which have the same form and the same location, and states of potential which differ between two initial images, a difference in the two initial images is produced pixel by pixel, according to the formula:

PC=(PA-PB)/2+INT(E/2)

in which PA is the value of the contrast level of the pixel of the first input image; PB is the value of the contrast level of the pixel of the second input image; E is the maximum value of the contrast level of the images; PC is the value of the contrast level of the pixel of the image formed; and INT is the whole part function.

31. A method as claimed in any one of claims 28 to 30, wherein, in order to form an image representing the common equipotential lines which are common to two initial images, there are carried out:

- a thresholding step, which adapts to three contrast levels , i.e. white, black and grey; and
- pixel by pixel, an extended AND+ intersection, during which the following contrast levels are allocated to each pixel of the image to be formed:
  - . black, if the two pixels of the initial images are black on completion of the adaptive thresholding;
  - . white, if the two pixels of the initial images are white on completion of the adaptive thresholding; and
  - . grey in all the other cases.

32. A method as claimed in any one of claims 28 to 31, wherein, in order to form an image which represents the equipotential lines of one or the other of two initial images, with the exclusion of the equipotential lines which are common to these two initial images, there are carried out:

Sub A9

- a thresholding step, which adapts to three contrast levels, i.e. white, black and grey; and
- pixel by pixel, an extended exclusive OR comparison, XOR+, during which the following contrast levels are allocated to each pixel of the image to be formed:
  - . grey, if the two pixels of the initial images have the same contrast value on completion of the adaptive thresholding;
  - . white, if the two pixels of the initial images are white and grey; or white and black; or grey and black, on completion of the adaptive thresholding; and
  - . black, if the two pixels of the initial images are black and grey; or black and white; or grey and white.

Sub B1

33. An installation for location of a fault of the short-circuit type, in a logic gate, known as the defective logic gate, of an integrated circuit, known as the defective circuit, comprising a chip for the input terminals and output terminals, which are connected to one another by electrically conductive tracks and logic gates formed within the chip of the circuit, which is generally in the form of a wafer defining a main plane of the chip, the tracks extending in the thickness of the chip or on the surface, globally parallel to the main plane, the input and output terminals being connected to the tracks at the periphery of the chip, and at least two electrical energy supply terminals with direct voltage (VDD-VSS), at least one supply terminal of which is connected to a high potential VDD, and at least one supply terminal of which is connected to a low potential VSS, the said installation comprising:

- means (10) for creating and recording a sequence of distinct vectors, known as location vectors, each of which is formed from a series of signals, which are designed to be able to be applied to the different input terminals of the defective circuit;
- equipotential imagery means (1), which, for at least one location vector applied to the input terminals of the defective circuit and/or of an integrated circuit, known as the standard circuit, which is free from a defective gate and from any fault, and is also identical to the defective circuit, can produce and record a set of images, known as vector images, representing equipotential lines formed by the tracks and the logic gates of the said circuit, each equipotential line corresponding to one of the differentiated states of potential on the vector images, the different vector images of a single set of images being designed to cover and represent the entire surface of the chip, or an entire portion of this surface on which it is being attempted to locate the defective logic gate,

wherein it comprises:

- means (10) for formation of a sequence of location vectors, in which each location vector is formed from binary signals which assume one of the logic states 0 and 1, and

maintain this logic state throughout an entire period, in which it is considered that the location vector is applied to the input terminals;

- means (11, 12) for applying the sequence of location vectors step by step to the input terminals of the defective circuit;
- for each location vector, means (23) for measurement of the value IDDQ(j) of the electrical consumption current at rest IDDQ of the defective circuit, which is circulating in at least one of the supply terminals;
- means (11) for calculation which can determine whether this value measured IDDQ(j) is normal or abnormal, and can record the result of this determination; and
- means (6) for calculation, which can make at least one comparison between at least one abnormal vector image (70, 76, 81, 89) and another pre-recorded image, known as the reference image (71, 77, 82, 88), corresponding to the same portion of surface of the chip of the defective circuit or of the standard circuit as the abnormal vector image, these images being selected such that this comparison makes it possible to select an area, known as the defective area, of the surface of the chip on which there can be located an equipotential input line (73) of the defective logic gate and/or an equipotential output line (74) of the defective logic gate, and/or the defective logic gate.

34. An installation as claimed in claim 33, wherein the means (23) for measurement of the value of the electrical consumption current at rest IDDQ of the circuit comprise an amplifier circuit (23) which is fitted as a current/voltage converter.

35. An installation as claimed in claim 34, wherein the amplifier circuit (23) fitted as a current/voltage converter is designed to create a virtual memory, which is adjustable according to the constraints imposed by the supply of the integrated circuit.